

**REMARKS**

At the time of the Office Action dated January 9, 2002, claims 1-13 were pending and rejected in this application. Claims 1-2, 8, 10-11, and 13 have been amended, and claim 5 has been cancelled. Care has been exercised to avoid the introduction of new matter. Specifically, claims 1 and 10 have been amended to modify the alternative recitation of the buried impurity region includes a recessed part or a gap part by deleting the recessed part from the recitation. As such, both claims 1 and 10 now recite that the buried impurity region includes a gap part. Claims 8 and 13 have been amended to correct antecedent basis issues arising from the amendments to claims 1 and 10. Applicant submits that the present Amendment does not generate any new matter issue.

Applicant notes that the Information Disclosure Statement and cited art filed April 16, 2001, were acknowledged by the Examiner on page two of the statement of the rejection. However, an initialed copy of the PTO-1449 form was not received. As such, Applicant hereby respectfully requests that the Examiner clarify the record by providing an appropriately initialed copy of the PTO-1449 form indicating consideration of the cited prior art.

**Claims 2-3 and 11 are rejected under the first paragraph of 35 U.S.C. § 112**

In the second enumerated paragraph of the Office Action, the Examiner asserted that claims 2-3 and 11 contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention. In particular, it is asserted that claims 2 and 11 recite that an electrode part is sandwiched between a third impurity

region and a semiconductor layer, but this is not shown in the drawings. This rejection is respectfully traversed.

Applicant notes that claims 2 and 11 have been amended to recite that an electrode part is formed over the first impurity region. Furthermore, claims 2 and 11 clarify that it is the first impurity region, and not the electrode part, that is sandwiched between the third impurity region and the semiconductor layer. Also, the insulating film is in between the electrode part and the first impurity region. As such, Applicant respectfully submits that the specification fully supports these limitations in such a way as to enable one skilled in the art to make and/or use the invention.

**Claims 1 and 5 are rejected under 35 U.S.C. § 103 for obviousness predicated upon Galbiati, et al., U.S. Patent No. 5,629,558 (hereinafter Galbiati), in view of Ludikhuize, EEE Publication**

In the second enumerated paragraph of the statement of the rejection, the Examiner asserted that Galbiati discloses all of the claimed structure except that the semiconductor element/diode explicitly includes a switching function and one having ordinary skill in the art would realize from Ludikhuize that the diode of Galbiati can have a switching function. This rejection is respectfully traversed.

Initially, Applicant notes that claim 1 has been amended to modify the recitation of alternative features for the second buried impurity region to only recite that "said second buried impurity region includes a first gap part wherein said second buried impurity region is

disconnected." This feature, for example, is shown in Fig. 7 of the drawings in which the second buried impurity region 4 is disconnected into two buried impurity regions 4a, 4b by a gap part in the second buried impurity region 4. By including a gap part in the second buried impurity region, the effective thickness of the semiconductor layer increases, which can improve the withstand voltage of the semiconductor device.

As such, Applicant respectfully submits that the Examiner cannot discharge the initial burden of establishing a prima facie basis to deny patentability to the claimed invention under 35 U.S.C. § 103. **In re Mayne**, 104 F.3d 1339, 41 USPQ2d 1451 (Fed. Cir. 1997); **In re Oetiker**, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In rejecting a claim under 35 U.S.C. § 103, the Examiner is required to identify a source in the applied prior art for: (1) claim limitations; and (2) the motivation to combine references or modify a reference in the reasonable expectation of achieving a particular benefit. **Smiths Industries Medical System v. Vital Signs Inc.**, 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999). In so doing, it is legally erroneous to ignore any claim limitation. **Uniroyal, Inc. v. Rudkin-Wiley Corp.**, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

The Examiner, on the last paragraph of page four of the Office Action, asserts that Galbiati discloses that the second buried impurity region 4 includes recessed parts 5. The recessed parts 5, however, do not extend completely through the second buried impurity region 4 of Galbiati; and therefore, the second buried impurity region 4 is not disconnected. Furthermore, neither Galbiati nor the secondary reference to Ludikhuizen provides any motivation to modify the recessed parts 5 to extend them completely through the second buried impurity region 4. As such, the combination of

Galbiati and Ludikhuize fails to teach or suggest that the second buried impurity region 4 includes a gap part in the second buried impurity region 4, as recited in claim 1.

It should, therefore, be apparent that the Examiner cannot discharge the initial burden of establishing a prima facie case of obviousness under 35 U.S.C. § 103. Applicant, therefore, respectfully submits that the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati in view of Ludikhuize is not factually or legally viable and, hence, solicits withdrawal thereof.

**Claims 4 and 9 are rejected under 35 U.S.C. § 103 for obviousness predicated upon Galbiati and Ludikhuize, as discussed above, and further in view of Terashima, U.S. Patent No. 5,874,767**

In the third enumerated paragraph of the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify the combination of Galbiati and Ludikhuize with Terashima to arrive at the claimed invention. This rejection is respectfully traversed.

Claims 4 and 9 depend ultimately from independent claim 1, and Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati and Ludikhuize. Specifically, the combination of Galbiati and Ludikhuize fails to teach or suggest that the second buried impurity region includes a gap part in the second buried impurity region that disconnects the second buried impurity region. The tertiary reference to Terashima does not cure the argued deficiencies of

Galbiati and Ludikhuize. Accordingly, the proposed combination of references would not yield the claimed invention because none of the applied references teach or suggest that the second buried impurity regions includes a gap part. **Uniroyal, Inc. v. Rudkin-Wiley Corp., supra**. Applicant, therefore, respectfully submits that the imposed rejection of claims 4 and 9 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati and Ludikhuize with Terashima is not factually or legally viable and, hence, solicits withdrawal thereof.

**Claims 6-8 are rejected under 35 U.S.C. § 103 for obviousness predicated upon the combination of Galbiati and Ludikhuize, as discussed above, and further in view of Singer, U.S. Patent No. 4,485,392**

In the fourth enumerated paragraph of the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to modify the combination of Galbiati and Ludikhuize with Singer to arrive at the claimed invention. This rejection is respectfully traversed.

Claims 6-8 depend ultimately from independent claim 1, and Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claim 1 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati and Ludikhuize. Specifically, the combination of Galbiati and Ludikhuize fails to teach or suggest that the second buried impurity region includes a gap part in the second buried impurity region that disconnects the second buried impurity region. The tertiary reference to Singer does not cure the argued deficiencies of Galbiati and Ludikhuize. Accordingly, the proposed combination of references would not yield the claimed invention because none of the applied references teach or suggest that the second buried impurity regions includes a

gap part. **Uniroyal, Inc. v. Rudkin-Wiley Corp., supra**. Applicant, therefore, respectfully submits that the imposed rejection of claims 6-8 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati and Ludikhuize with Singer is not factually or legally viable and, hence, solicits withdrawal thereof.

**Claims 10 and 12-13 are rejected under 35 U.S.C. § 103 for obviousness predicated upon the combination of Galbiati, Ludikhuize, Singer, and Harris, U.S. Patent No. 6,127,695**

In the fifth enumerated paragraph of the statement of the rejection, the Examiner asserted that one having ordinary skill in the art would have been motivated to combine Galbiati, Ludikhuize, and Singer with Harris to arrive at the claimed invention. This rejection is respectfully traversed.

Applicant notes that claim 10 has been amended to modify the recitation of alternative features for the buried impurity region to only recite that "said buried impurity region includes a gap part wherein said buried impurity region is disconnected." By including a gap part in the buried impurity region, the effective thickness of the semiconductor layer increases, which can improve the withstand voltage of the semiconductor device.

The Examiner, while referring to the Examiner's discussion of claim 1, asserts that Galbiati discloses that the buried impurity region 4 includes recessed parts 5. The recessed parts 5, however, do not extend completely through the buried impurity region 4 of Galbiati; and therefore, the buried impurity region 4 is not disconnected. Furthermore, neither Galbiati nor the secondary references to

Ludikhuize, Singer, and Harris provide any motivation to modify the recessed parts 5 to extend them completely through the buried impurity region 4. As such, the combination of Galbiati and Ludikhuize, Singer, and Harris fails to teach or suggest that the buried impurity region 4 includes a gap part in the buried impurity region 4, as recited in claim 10.

It should, therefore, be apparent that the Examiner cannot discharge the initial burden of establishing a prima facie case of obviousness under 35 U.S.C. § 103. Applicant, therefore, respectfully submits that the imposed rejection of claims 10 and 12-13 under 35 U.S.C. § 103 for obviousness predicated upon Galbiati in view of Ludikhuize is not factually or legally viable and, hence, solicits withdrawal thereof.

Under 37 C.F.R. § 1.104(c), the Examiner is required to "cite the best references at his or her command," and since the Examiner was also obligated to reject each claim on all valid grounds available, see M.P.E.P. § 707.07(g), Applicant can therefore conclude that the Examiner has already set forth the best rejections possible over the applied references.

Moreover, since the Examiner's first search should have covered the invention as described in the specification, as well as the invention claimed and the inventive concepts toward which the claims appear to be directed, see, e.g., M.P.E.P. § 904, consistent with the mandate to give the claims the broadest reasonable interpretation during prosecution and the mandate to avoid "piecemeal" prosecution to thereby enable Applicant with a full and fair hearing and to clearly develop any issues prior to appeal, it is believed that the claimed invention is patentable over any possible combination of the applied references. See, e.g., In re Morris, 127 F.3d 1048 (Fed. Cir. 1997);

M.P.E.P. § 706.07. Since the amendments herein clearly lie within the subject matter already disclosed to the Examiner within Applicant's original specification, these amendments do not raise new issues.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

Applicant has made every effort to present claims which distinguish over the prior art, and it is believed that all claims are in condition for allowance. However, Applicant invites the Examiner to call the undersigned if it is believed that a telephonic interview would expedite the prosecution of the application to an allowance. Accordingly, and in view of the foregoing remarks, Applicant hereby respectfully requests reconsideration and prompt allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417, and please credit any excess fees to such deposit account.

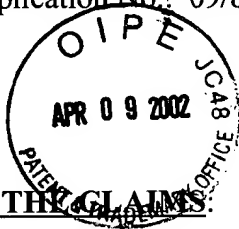
Respectfully submitted,

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Version with markings to show changes made

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IN THE CLAIMS:

1. (Amended) A semiconductor device including:
    - a semiconductor substrate having a main surface;
    - a semiconductor layer of a first conductive type which is formed on the main surface of said semiconductor substrate;
    - a first buried impurity region of the first conductive type formed between said semiconductor layer and said semiconductor substrate;
    - a second buried impurity region of a second conductive type formed between said first buried impurity region and said semiconductor layer;
    - a first impurity region of the second conductive type which is formed in the surface of said semiconductor layer and which is electrically connected to said second buried impurity region;
    - a second impurity region of the first conductive type which is formed in the surface or inside of said semiconductor layer located in a region above said second buried impurity region;
    - and
    - a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,wherein the withstanding voltage is secured by a depletion layer extending from an interface between said second buried impurity region and said semiconductor layer under the condition where said semiconductor element is turned OFF; and
  - said second buried impurity region includes [a first recessed part wherein a surface of said second buried impurity region is recessed in the direction away from said second impurity region in a part located, approximately, directly beneath said second impurity region or] a first gap part wherein said second buried impurity region is disconnected.
2. (Amended) The semiconductor device according to claim 1, wherein said semiconductor element includes:

a third impurity region of the first conductive type formed on the surface of said first impurity region so as to be surrounded by said first impurity region; and

an electrode part formed [on the surface of] over said first impurity region, said first impurity region sandwiched between said third impurity region and said semiconductor layer with an insulating film [interpolated] in between the electrode part and the first impurity region.

Please cancel claim 5 in its entirety without prejudice or disclaimer of the subject matter thereof.

8. (Amended) The semiconductor device according to claim 1, wherein said first buried impurity region includes a [second] recessed part wherein a surface of said first buried impurity region is recessed in the direction away from said second impurity region in a part located, approximately, directly beneath said first gap part or a second gap part wherein said first buried region is disconnected.

10. (Amended) A semiconductor device including:  
a semiconductor substrate having a main surface;  
a semiconductor layer of a first conductive type formed on the main surface of said semiconductor substrate;  
a buried impurity region of the first conductive type formed between said semiconductor substrate and said semiconductor layer;  
a first impurity region of the first conductive type which is formed on the surface of said semiconductor layer and which is electrically connected to said buried impurity region;  
a second impurity region of a second conductive type formed on a surface of said semiconductor layer located in a region above said buried impurity region; and  
a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,  
wherein a withstanding voltage is secured by a depletion layer extending from an interface between said second impurity region and said semiconductor layer under the condition where said semiconductor element is turned off; and

said buried impurity region includes [a recessed part wherein a surface of said buried impurity region is recessed in the direction away from said second impurity region in a part located, approximately, directly beneath said second impurity region or] a gap part wherein said buried region is disconnected.

11. (Amended) The semiconductor device according to claim 10, wherein said semiconductor element includes:

a third impurity region of the first conductive type formed on a surface of said second impurity region so as to be surrounded by said second impurity region; and

an electrode part formed [on a surface of] over said second impurity region, said first impurity region sandwiched by said third impurity region and said semiconductor layer with an insulating film [interpolated] in between the electrode part and the first impurity region.

13. (Amended) The semiconductor device according to claim 10, wherein said [recessed part or] gap part is formed in a part that is in the direction to which said depletion layer extends.